



晶片鋁墊與打線腳位對應表

Pad Location Information

<i>Product Description</i>	
<i>Device Name</i>	__GDS6606ACP6__
<i>Mask ID</i>	__BK2046A*__ (*代表 A-Z 共用版本,僅適用在 Pad 位置相同)
<i>Requirement</i>	<input type="checkbox"/> Tapeout 前 try bonding(封裝廠僅評估能否拉線) <input checked="" type="checkbox"/> Tapeout 後 ENG bonding diagram(封裝廠須出 BD 圖)
<i>Package Type & Size</i>	Package Type: CPC -20 L *(<input type="text"/> x <input type="text"/> x <input type="text"/> 膠體厚度) *L/F Pin Pitch: <input type="text"/>
<i>Material type</i>	L/F Pad Size: <input type="text"/> x <input type="text"/> (SOP / TSOP / TSSOP / MSOP: <input type="checkbox"/> Normal <input type="checkbox"/> Exposed) Compound: Green
<i>Die Size</i>	<input type="text"/> 1490 μm x <input type="text"/> 1520 μm (Scribe Line: <input type="text"/> 60 μm)
<i>Wafer Size</i>	<input type="text"/> 8 Inch
<i>Material Description</i>	
<i>Wafer Substrate</i>	<input checked="" type="checkbox"/> P-Sub <input type="checkbox"/> N-Sub
<i>Die Bond Material</i>	<input checked="" type="checkbox"/> Conductive <input type="checkbox"/> Non-conductive <input type="checkbox"/> Other:
<i>Wire</i>	<input type="checkbox"/> Au 1.0mil <input type="checkbox"/> Cu 1.0mil <input checked="" type="checkbox"/> Other: _Cu 0.8_mil (備註:)
<i>Metal Layer</i>	Total <input type="text"/> 4 layer, Top metal thickness: <input type="text"/> 3.2(ThinM4/M3/M2)_ μm
<i>Circuit under bond pad</i>	<input type="checkbox"/> No <input checked="" type="checkbox"/> Yes
<i>Foundry</i>	FAB: <input type="text"/> SKHynix
<i>Metallization</i>	Al <input type="text"/> 98 % & Cu <input type="text"/> 1.5 % & Si <input type="text"/> 0.5 %
<i>Specially Bonding Note</i>	

Unit : μm

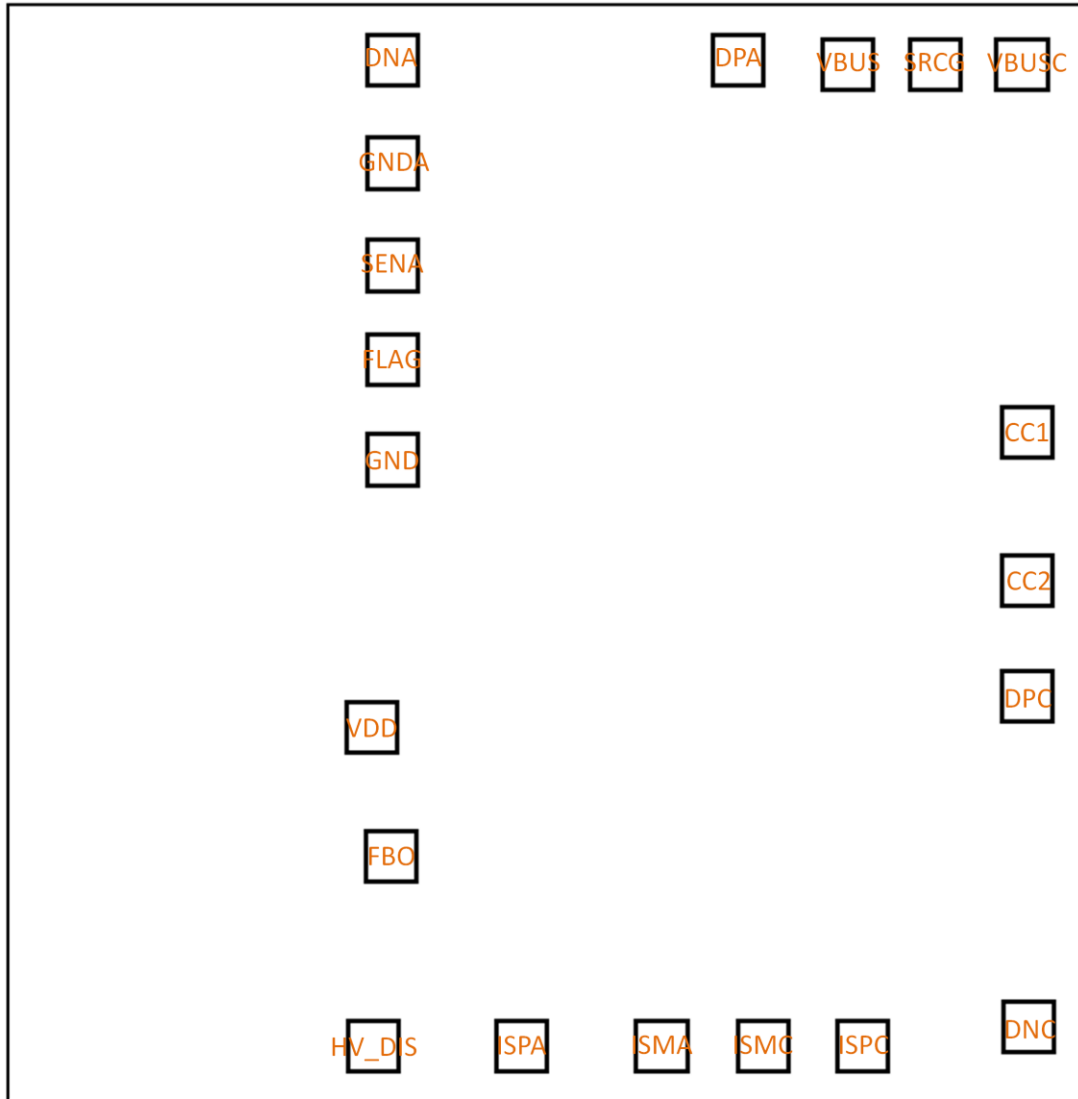
Bond Pad Name	Ball Center (X,Y)	Pad Center (X,Y)	Pad Size (X,Y)	L/F Pin Out Number	Bond Pad Name	Ball Center (X,Y)	Pad Center (X,Y)	Pad Size (X,Y)	L/F Pin Out Number
GNDA		(-212.6,540.7)	(70,70)	3	ISPC		(436.5,-681.3)	(70,70)	13
SENA		(-212.6,399)	(70,70)	4	DNC		(666.3,-654.3)	(70,70)	14
FLAG		(-213.2,269.2)	(70,70)	5	DPC		(664.3,-196.8)	(70,70)	15
GND		(-213.2,130.4)	(70,70)	6	CC2		(664.3,-37.1)	(70,70)	16
VDD		(-242.5,-239.3)	(70,70)	7	CC1		(664.3,168.5)	(70,70)	17
FBO		(-215.6,-418.6)	(70,70)	8	VBUSC		(657.5,677.4)	(70,70)	18
HV_DIS		(-239.6,-681.3)	(70,70)	9	SRCG		(537.1,677.4)	(70,70)	19
ISPA		(-34.5,-681.3)	(70,70)	10	VBUS		(416.8,677.4)	(70,70)	20
ISMA		(159,-681.3)	(70,70)	11	DPA		(264.5,682.3)	(70,70)	1



ISMC		(298.8,-681.3)	(70,70)	12	DNA		(-212.6,682.3)	(70,70)	2

Bond Pad LAYOUT of Chip

附件一





Brief 打線示意圖

附件二

